

**S/N 09/808,750**

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant:	Huy T. Vo	Examiner:	Son Mai
Serial No.:	09/808,750	Group Art Unit:	2827
Filed:	March 15, 2001	Docket:	303.723US1
Title:	DEVICE AND METHOD TO REDUCE WORDLINE RC TIME CONSTANT IN SEMICONDUCTOR MEMORY DEVICES		

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**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

Mail Stop AF  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

The Applicant requests review of the final rejection in the above-identified application.  
No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested because Applicant believes a *prima facie* case of anticipation under 35 U.S.C. § 102(b) has not been shown.

**Rejections under 35 U.S.C. § 102(b)**

All of the claims at issue, namely claims 1-41 and 45-57, were rejected under 35 U.S.C. § 102(b) as being anticipated by Cowles (U.S. Patent No. 5,940,315, hereinafter “Cowles”). This rejection is respectfully traversed. Applicant respectfully submits that the Final Office Action of January 30, 2006 has not made a proper *prima facie* showing of anticipation at least because Cowles fails to teach each and every element recited or incorporated into claims 1-41 and 45-57.

*Regarding claims 1-4:*

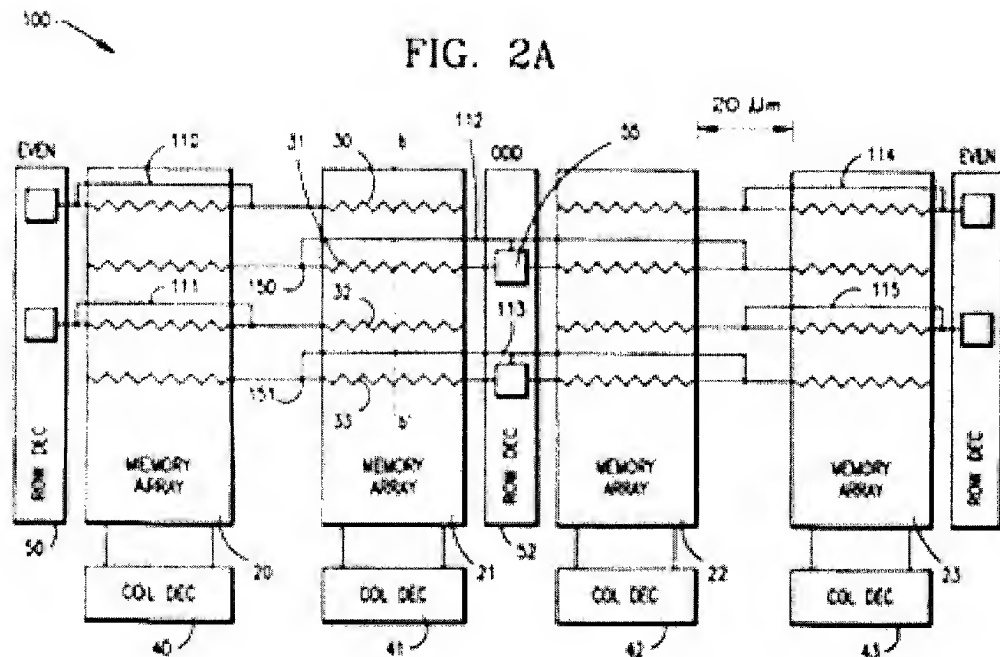
Applicant cannot find in Cowles, among other things,

a strapping line of lower resistance than the wordlines coupled to a single continuous wordline in a single array wherein the strapping line bypasses only a portion in a middle region between a first and second end of the single continuous wordline, ..., and wherein the strapping line bypasses only a portion of a wordline within the single array and bypasses a different portion of a wordline within the single array than an adjacent strapping line,

as recited in claim 1 or incorporated in claims 2-4. The conductive straps of Cowles bypass a wordline across an entire memory array (see e.g., FIG. 2A of Cowles reproduced below), instead

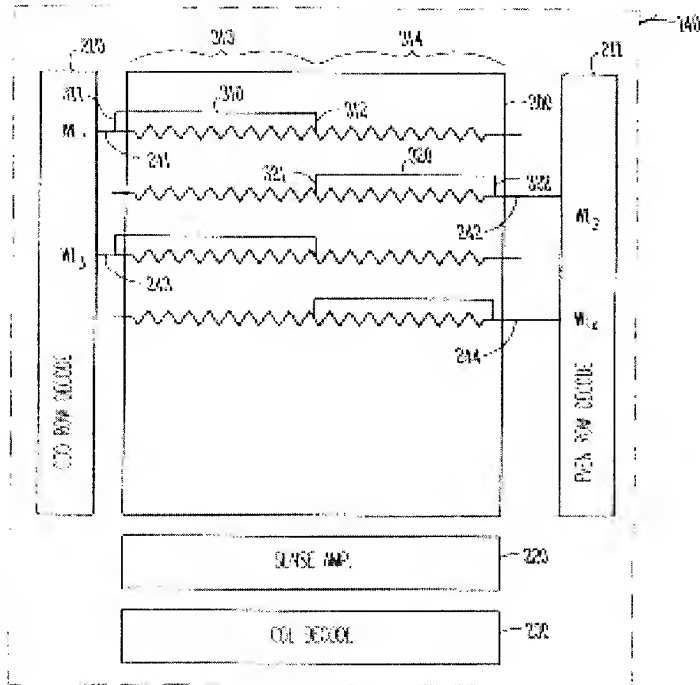
of only a portion of a wordline within the single array as recited in claim 1. The Final Office Action asserts that the memory bank 100 of Cowles reads on the single memory array recited in claim 1 (*see* Final Office Action pg. 3), and apparently asserts that because Cowles shows metal straps spanning wordlines of the memory arrays within the memory bank Cowles therefore bypasses a different portion of a wordline within the memory array.

However, the memory bank 100 of Cowles is made of more than one memory array (*see* FIG. 2A), and Cowles states that the invention ... may be used with any number of arrays greater than one (*see* col. 3 lines 23-27). Cowles also states that “[s]traps 112, 113 are connected to wordlines 31, 33 respectively outside the edge of [memory] array 21 as shown in FIG. 2A at nodes 150, 151 through a contact hole in the poly layers” (*see* Cowles, col. 4 lines 2-4). Thus, Cowles does not disclose the structure recited in claim 1.



Claims 5-41 and 45-54 recite or incorporate the limitations of a number of wordlines and strapping lines or devices to bypass only a portion of the wordlines within a memory array. An example of strapping lines bypassing only a portion of the wordlines within a memory is shown

in FIG. 5 of the present application (reproduced below).



*Fig. 5*

Thus Cowles does not disclose the structure recited or incorporated in the claims. For example, Cowles does not contain any disclosure of “wherein adjacent strapping lines bypass only a portion of a wordline within the memory array”, or any disclosure of “[wherein adjacent strapping lines] bypass different portions of adjacent wordlines within the memory array,” as recited in claim 5.

Additionally, Claim 55 recites

an even row decoder located on a first side of the memory array, an odd row decoder located on a second side of the memory array, ... wherein a strapping line connected to an odd wordline bypasses only a portion of the odd wordline within the memory array nearer the odd row decoder, wherein a strapping line connected to an even wordline bypasses only a portion of the even wordline within the memory array nearer the even row decoder.

Cowles describes,

“[r]ow decoders 50 and 54 are designated as even row decoders, and row decoder 52 is designated as an odd row decoder. Row decoder 50 is positioned adjacent to memory array 20 on the opposite side of memory array 21, row decoder 52 is positioned between memory array 21 and memory array 22 and row decoder 54 is positioned adjacent to memory array 23 on the opposite side of memory array 22 as shown”

(see Cowles, FIG. 2A and col. 3 lines 39-46). Thus, Cowles refers to an arrangement where an even row decoder is on one side of two memory arrays and an odd row decoder is on an opposite side of the two memory arrays, and therefore Cowles does not describe the structure recited in claim 55 and incorporated into claims 56 and 57.

In summary, neither the Final Office Action dated January 30, 2006 or the Advisory Action dated April 14, 2006, set forth a proper *prima facie* case of anticipation with respect to the claims because each and every element as set forth in claims 1-41 and 45-57 is not found, either expressly or inherently described, in Cowles. Cowles does not disclose the structure recited or incorporated into the claims at issue. Therefore, Applicant requests reversal of the 35 U.S.C. § 102(b) rejection and allowance of claims 1-41 and 45-57.

**CONCLUSION**

The applicant respectfully submits that all of the pending claims are in condition for allowance, and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at (612) 349-9587 to discuss any questions which may remain with respect to the present application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

HUY T. VO


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Date

30 April '06

By



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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 30 day of April, 2006.

Name

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Signature

